REMARKS

Claims 1-27 were examined, with all claims rejected.

Specification and Claim Objections

The disclosure and claims 11, 15, and 21 are objected to because of informalities. Applicant has amended the specification and these claims in accordance with the Examiner's suggestions, and thus these objections are believed to be overcome.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 4, 6, 7, 12, 14, and 16 are rejected under 35 U.S.C. § 102(e) as being anticipated by Struhsaker et al. (U.S. Patent No. 6,128,331). Claims 1, 3, 12, and 15 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shiue et al. (U.S. Patent No. 6,590,872). Claims 1, 8-10, 12, 18, 19, and 21-26 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kohli et al. (U.S. Patent No. 6,393,046). Claims 1, 2, 5, 8, 11-14, 16, 19, 20, 23, and 27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Buehrer et al. (U.S. Patent No. 6,549,565).

While not conceding the validity of any of these rejections, Applicant has amended claims 6, 17, 18, and 26 to be in independent form, and has canceled claims 1-5, 7-16, 19-25, and 27. Applicant has also added new claim 28.

Claims 6 and 17:

Claims 6 and 17 are directed to a searcher device and method that correlates a first code sequence with a second code sequence. The searcher has a memory, which stores the first code sequence, and computation circuits. Each of the computation circuits performs a correlation operation between the first code sequence and the second code sequence at a unique phase offset, and has a unique coupling offset from each other with respect to a location in which they are coupled to the memory.

None of the applied references, including Struhsaker, teaches computation circuits that have a unique coupling offset from each other with respect to a location in which they are coupled to a memory, as required by claims 6 and 17.

Struhsaker is directed to a correlation system for use in wireless direct sequence spread spectrum systems that includes a RF down converter which receives an encoded RF signal and generates therefrom analog in-phase (I) and quadrature (Q) signal components. These components are digitized and the digitized signals are then passed to each of the high precision correlator circuit and a low precision correlator circuit. The low precision correlator circuit consists of a bank of a plurality of low precision correlators which receive the I and Q signal components as inputs and correlate the same with progressively phase shifted or delay pseudo noise (PN) codes. A low precision correlation circuit locks on to the appropriate PN code phase shift or delay and applies the same as a reference PN code to the high precision correlation circuit for data acquisition and demodulization.

Struhsaker has no disclosure of a memory, not to mention how the correlators are coupled thereto. The figure shows that correlators 28 are connected to a precision conversion 26, and in col. 3, lines 33-35, Struhsaker merely states that "The circuit 26 is operative to convert the I and Q signals to a format suitable for receipt and operation by the low precision correlation circuit 20 ... ." Again, there is no discussion as to how these correlators are connected to any memory. There is therefore no disclosure of computation circuits that have a unique coupling offset from each other with respect to a location in which they are coupled to a memory, as required by claims 6 and 17. Thus, claims 6 and 17 are patentable over the applied references.

Claims 18 and 26:

Claim 18 is directed to a method of determining a phase offset of a signal. In the method, the signal having a first code sequence is received in a memory, and an additional signal having a second code sequence is received at a plurality of computation circuits. A unique phase offset for the second code sequence is implemented in each of the plurality of computation circuits by temporarily storing the second code sequence in a memory buffer with varying size to provide the unique phase offset to each of the plurality of computation circuits. And the second code sequence having the unique phase offsets is correlated with the first code sequence in each of the respective plurality of computation circuits.

Similarly, claim 26 is directed to a data signal processing communication device having a transceiver for receiving a signal having a first code sequence, a code generator for generating a second code sequence, a searcher coupled to the transceiver and to the code generator, wherein the searcher has computation circuits that correlate in parallel the first code sequence and the second code sequence at a plurality of offsets, and a memory block coupled to one of the computation circuits, wherein the memory block has a variable length to implement a variable offset between the first code sequence and the second code sequence.

Kohli does not teach temporarily storing the second code sequence in a memory buffer with varying size, as required by claim 18, or a memory block coupled to one of the computation circuits and having a variable length, as required by claim 26.

Kohli is directed to GPS navigation systems such as those used in terrestrial navigation for cars, trucks, and other land vehicles. Unlike the present invention, Kohli does not relate to searchers of communication systems. In any event, the Examiner refers applicant to col. 18, lines 12-14, which state that "It is convenient to use ½ chip delays for each delay 78, but other fractions of a chip width may be used." This sentence does not state that a memory buffer or block is of varying size, as required by claims 18 and 26. Immediately prior to this sentence in col. 18, lines 1-3, Kohli states that "... an expanded series of correlations are performed with a series of delays in a

fixed fraction of a chip width ..." (emphasis added). It is thus clear that the sentence to which the Examiner refers is stating that while different fractions of a chip are options, the chosen option is fixed. Thus, Kohli does not teach a buffer or memory block of varying size, as required by claims 18 and 26.

New claim 28:

Applicant has added new independent claim 28, which is directed to a searcher device for correlating a first code sequence with a second code sequence. The searcher has a memory for storing the first code sequence, a plurality of computation circuits coupled to the memory, and a plurality of offset code sequence generators that are coupled respectively to the plurality of computation circuits and generate the second code sequence at unique phase offsets, wherein each of the plurality of computation circuits performs a correlation operation between the first code sequence and the second code sequence at a unique phase offset. By having the plurality of offset code sequence generators that are coupled respectively to the plurality of computation circuits and generate the second code sequence at unique phase offsets, each of the plurality of computation circuits has a separate input. As discussed on page 12 of the specification, since each circuit has a separate input, no memory buffer is required for coupling input signals to the computation circuits. Claim 28 is believed to be patentable over the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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